Amendment of Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (currently amended) A charge pump type DC/DC converter ~~having the following~~ comprising:

a voltage input terminal connected to the output terminal of a DC power supply;

first and second capacitors;

a voltage output terminal connected to a load;

a switch circuit network having a first phase, in which a first terminal of the ~~aforementioned~~ first capacitor is connected to the ~~aforementioned~~ voltage input terminal, a first terminal of the ~~aforementioned~~ second capacitor is connected to the ~~aforementioned~~ voltage output terminal, and a second terminal of the first capacitor and a second terminal of the second capacitor are connected to each other, and a second phase, in which the first and second terminals of the ~~aforementioned~~ first capacitor are connected to the ~~aforementioned~~ voltage output terminal and the voltage input terminal, respectively, and the first and second terminals of the second capacitor are connected to the ~~aforementioned~~ voltage input terminal and a reference potential, respectively; and

a switching ~~control means~~ controller that controls the ~~aforementioned~~ switch circuit network to switch the ~~aforementioned~~ first and second phases alternately at prescribed duty ratios.

2. (currently amended) The DC/DC converter described in Claim 1 ~~characterized by the fact that~~ wherein the first capacitor is a one capacitor element.

3. (currently amended) The DC/DC converter described in Claim 2 ~~characterized by the fact that~~ wherein the capacitance of the first capacitor is approximately equal to that of the second capacitor.

4. (currently amended) The DC/DC converter described in any of ~~Claims 1-3 characterized by the fact that~~ Claim 1 wherein the duty ratios of the ~~aforementioned~~ first and second phases are set at about ½.

5. (currently amended) The DC/DC converter described in ~~any of Claims 1-4 characterized by the following facts:~~ Claim 1 wherein

the ~~aforementioned~~ switch circuit network ~~has the following:~~ comprises:

a first MOS transistor with a first terminal connected to the ~~aforementioned~~ voltage input terminal and a second terminal connected to the first terminal of the ~~aforementioned~~ first capacitor;

a second MOS transistor with a first terminal connected to the ~~aforementioned~~ voltage input terminal and a second terminal connected to the second terminal of the ~~aforementioned~~ first capacitor;

a third MOS transistor with a first terminal connected to the ~~aforementioned~~ voltage input terminal and a second terminal connected to the first terminal of the ~~aforementioned~~ second capacitor;

a fourth MOS transistor with a first terminal connected to the second terminal of the ~~aforementioned~~ first capacitor and a second terminal connected to the second terminal of the ~~aforementioned~~ second capacitor;

a fifth MOS transistor with a first terminal connected to the second terminal of the ~~aforementioned~~ second capacitor and a second terminal connected to the ~~aforementioned~~ reference potential;

a sixth MOS transistor with a first terminal connected to the first terminal of the ~~aforementioned~~ first capacitor and a second terminal connected to the ~~aforementioned~~ voltage output terminal; and

a seventh MOS transistor with a first terminal connected to the first terminal of the ~~aforementioned~~ second capacitor and a second terminal connected to the ~~aforementioned~~ voltage output terminal;

~~the aforementioned switching control means controls as follows:~~

in the first phase, the switching controller keeps the ~~aforementioned~~ first, fourth, and seventh MOS transistors ~~are kept~~ in the on state, and the ~~aforementioned~~ second, third, fifth, and sixth MOS transistors ~~are kept~~ in the off state; and wherein

in the second phase, the switching controller keeps the ~~aforementioned~~ first, fourth, and seventh MOS transistors are kept in the off state, and the ~~aforementioned~~ second, third, fifth, and sixth MOS transistors ~~are kept~~ in the on state.

6. (currently amended) The DC/DC converter described in Claim 1 ~~characterized by the fact that~~ wherein the ~~aforementioned~~ first capacitor is comprised of n (n is an integer of 2 or larger) capacitor elements, the ~~aforementioned~~ n capacitor elements are connected in series in the ~~aforementioned~~ first phase, and the ~~aforementioned~~ n capacitor elements are connected in parallel with each other in the ~~aforementioned~~ second phase.

7. (currently amended) The DC/DC converter described in Claim 6 ~~characterized by the fact that~~ wherein the ~~aforementioned~~ n capacitor elements have approximately the same capacitance.

8. (currently amended) The DC/DC converter described in Claim 6 ~~or 7 characterized by the fact that~~ wherein the duty ratio of the ~~aforementioned~~ first phase is set at about 1/(n+1), and the duty ratio of the ~~aforementioned~~ second phase is set at about n/(n+1).

9. (currently amended) The DC/DC converter described in ~~any of Claims 6-8 characterized by the following facts:~~ Claim 6 wherein the ~~aforementioned~~ first capacitor is comprised of first and second capacitor elements~~;~~ and the ~~aforementioned~~ switch circuit network ~~has the following:~~comprises:

a first MOS transistor with a first terminal connected to the ~~aforementioned~~ voltage input terminal and a second terminal connected to the first terminal of the ~~aforementioned~~ first capacitor element;

a second MOS transistor with a first terminal connected to the ~~aforementioned~~ voltage input terminal and a second terminal connected to the second terminal of the ~~aforementioned~~ first capacitor element;

a third MOS transistor with a first terminal connected to the second terminal of the ~~aforementioned~~ first capacitor element and a second terminal connected to the first terminal of the ~~aforementioned~~ second capacitor element;

a fourth MOS transistor with a first terminal connected to the ~~aforementioned~~ voltage input terminal and a second terminal connected to the second terminal of the ~~aforementioned~~ second capacitor element;

a fifth MOS transistor with a first terminal connected to the ~~aforementioned~~ voltage input terminal and a second terminal connected to the first terminal of the ~~aforementioned~~ second capacitor;

a sixth MOS transistor with a first terminal connected to the second terminal of the ~~aforementioned~~ second capacitor element and a second terminal connected to the second terminal of the ~~aforementioned~~ second capacitor;

a seventh MOS transistor with a first terminal connected to the second terminal of the ~~aforementioned~~ second capacitor and a second terminal connected to the ~~aforementioned~~ reference potential;

an eighth MOS transistor with a first terminal connected to the first terminal of the ~~aforementioned~~ first capacitor element and a second terminal connected to the ~~aforementioned~~ voltage output terminal;

a ninth MOS with a first terminal connected to the first terminal of the ~~aforementioned~~ second capacitor element and a second terminal connected to the ~~aforementioned~~ voltage output terminal; and

a tenth MOS transistor with a first terminal connected to the first terminal of the ~~aforementioned~~ second capacitor and a second terminal connected to the ~~aforementioned~~ voltage output terminal;

~~the aforementioned switching control means controls as follows:~~

in the first phase, the switching controller keeps the first, third, sixth, and tenth MOS transistors ~~are kept~~ in the on state, and the second, fourth, fifth, seventh, eighth, and ninth MOS transistors ~~are kept~~ in the off state;

wherein in the second phase, the switching controller keeps, the first, third, sixth, and tenth MOS transistors ~~are kept~~ in the off state, and the second, fourth, fifth, seventh, eighth, and ninth MOS transistors ~~are kept~~ in the on state.

10. (currently amended) The DC/DC converter described in Claim 1 ~~characterized by the fact that~~ wherein the ~~aforementioned~~ first capacitor is comprised of n (n is an integer of 2 or larger) capacitor elements, the ~~aforementioned~~ n capacitor elements are connected in parallel with each other in the ~~aforementioned~~ first phase, and the ~~aforementioned~~ n capacitor elements are connected in series in the ~~aforementioned~~ second phase.

11. (currently amended) The DC/DC converter described in Claim 10 ~~characterized by the fact that~~ wherein the ~~aforementioned~~ n capacitor elements have approximately the same capacitance.

12. (currently amended) The DC/DC converter described in Claim 10 ~~or 11 characterized by the fact that~~ wherein the duty ratio of the ~~aforementioned~~ first phase is set at about n/(n+1), and the duty ratio of the ~~aforementioned~~ second phase is set at about 1/(n+1).

13. (currently amended) The DC/DC converter described ~~in any of Claims 10-12 characterized by the following facts:~~ Claim 10 wherein the ~~aforementioned~~ first capacitor is comprised of first and second capacitor elements; the ~~aforementioned~~ switch circuit network has the following:

a first MOS transistor with a first terminal connected to the ~~aforementioned~~ voltage input terminal and a second terminal connected to the first terminal of the ~~aforementioned~~ first capacitor element;

a second MOS transistor with a first terminal connected to the second terminal of the first MOS transistor and a second terminal connected to the first terminal of the ~~aforementioned~~ second capacitor element;

a third MOS transistor with a first terminal connected to the second terminal of the ~~aforementioned~~ first capacitor element and a second terminal connected to the first terminal of the ~~aforementioned~~ second capacitor element;

a fourth MOS transistor with a first terminal connected to the ~~aforementioned~~ voltage input terminal and a second terminal connected to the second terminal of the ~~aforementioned~~ second capacitor element;

a fifth MOS transistor with a first terminal connected to the second terminal of the ~~aforementioned~~ first capacitor element and a second terminal connected to the second terminal of the ~~aforementioned~~ second capacitor element;

a sixth MOS transistor with a first terminal connected to the ~~aforementioned~~ voltage input terminal and a second terminal connected to the first terminal of the ~~aforementioned~~ second capacitor;

a seventh MOS transistor with a first terminal connected to the second terminal of the ~~aforementioned~~ second capacitor element and a second terminal connected to the second terminal of the ~~aforementioned~~ second capacitor;

an eighth MOS transistor with a first terminal connected to the second terminal of the ~~aforementioned~~ second capacitor and a second terminal connected to the ~~aforementioned~~ reference potential;

a ninth MOS transistor with a first terminal connected to the first terminal of the first capacitor element and a second terminal connected to the ~~aforementioned~~ voltage output terminal; and

a tenth MOS transistor with a first terminal connected to the first terminal of the ~~aforementioned~~ second capacitor and a second terminal connected to the ~~aforementioned~~ voltage output terminal;

~~the aforementioned switching control means controls as follows:~~

in the first phase, the switching controller keeps the ~~aforementioned~~ first, second, fifth, seventh, and tenth MOS transistors ~~are kept~~ in the on state, and the ~~aforementioned~~ third, fourth, sixth, eighth, and ninth MOS transistors ~~are kept~~ in the off state; and wherein

in the second phase, the switching controller keeps the ~~aforementioned~~ first, second, fifth, seventh, and tenth MOS transistors ~~are kept~~ in the off state, and the ~~aforementioned~~ third, fourth, sixth, eighth, and ninth MOS transistors ~~are kept~~ in the on state.

14. (currently amended) The DC/DC converter described in Claim 1 ~~characterized by the following facts:~~ the ~~aforementioned~~ first capacitor is comprised of ~~nxm~~ n x m (n and m are integers of 2 or larger) capacitor elements; in the first phase, for the ~~aforementioned~~ nxm capacitor elements, all n capacitor elements are connected in series, and these serial capacitor circuits are connected in parallel in m columns; in the second phase, for the ~~aforementioned~~ ~~nxm~~ n x m capacitor elements, all m capacitor elements are connected in series, and these serial capacitor circuits are connected in parallel in n columns.

15. (currently amended) The DC/DC converter described in Claim 14 ~~characterized by the fact that~~ wherein the ~~aforementioned~~ ~~nxm~~ n x m capacitors have approximately the same capacitance.

16. (currently amended) The DC/DC converter described in Claim 14 ~~or 15 characterized by the fact that~~ wherein the duty ratio of the first phase is set at about m/(n+m), and the duty ratio of the ~~aforementioned~~ second phase is set at about n/(n+m).

17. (currently amended) The DC/DC converter described in ~~any of Claims 14-16 characterized by the following facts:~~ Claim 14 wherein the ~~aforementioned~~ first capacitor is comprised of first, second, third, and fourth capacitor elements; the ~~aforementioned~~ switch circuit network ~~has the following~~ comprises:

a first MOS transistor with a first terminal connected to the ~~aforementioned~~ voltage input terminal and a second terminal connected to the first terminal of the ~~aforementioned~~ third capacitor element;

a second MOS transistor with a first terminal connected to the first terminal of the ~~aforementioned~~ third capacitor element and a second terminal connected to the first terminal of the ~~aforementioned~~ first capacitor element;

a third MOS transistor with a first terminal connected to the ~~aforementioned~~ voltage input terminal and a second terminal connected to the second terminal of the ~~aforementioned~~ first capacitor element;

a fourth MOS transistor with a first terminal connected to the second terminal of the ~~aforementioned~~ first capacitor element and a second terminal connected to the first terminal of the ~~aforementioned~~ second capacitor element;

a fifth MOS transistor with a first terminal connected to the ~~aforementioned~~ voltage input terminal and a second terminal connected to the second terminal of the ~~aforementioned~~ second capacitor element;

a sixth MOS transistor with a first terminal connected to the second terminal of the ~~aforementioned~~ third capacitor element and a second terminal connected to the first terminal of the ~~aforementioned~~ fourth capacitor element;

a seventh MOS transistor with a first terminal connected to the first terminal of the ~~aforementioned~~ first capacitor element and a second terminal connected to the second terminal of the ~~aforementioned~~ third capacitor element;

an eighth MOS transistor with a first terminal connected to the first terminal of the ~~aforementioned~~ second capacitor element and a second terminal connected to the second terminal of the ~~aforementioned~~ fourth capacitor element;

a ninth MOS transistor with a first terminal connected to the second terminal of the ~~aforementioned~~ second capacitor element and a second terminal connected to the second terminal of the ~~aforementioned~~ fourth capacitor element;

a tenth MOS transistor with a first terminal connected to the ~~aforementioned~~ voltage input terminal and a second terminal connected to the first terminal of the ~~aforementioned~~ second capacitor;

an eleventh MOS transistor with a first terminal connected to the second terminal of the ~~aforementioned~~ fourth capacitor element and a second terminal connected to the second terminal of the ~~aforementioned~~ second capacitor;

a twelfth MOS transistor with a first terminal connected to the second terminal of the ~~aforementioned~~ second capacitor and a second terminal connected to the ~~aforementioned~~ reference potential;

a thirteenth MOS transistor with a first terminal connected to the first terminal of the ~~aforementioned~~ third capacitor element and a second terminal connected to the ~~aforementioned~~ voltage output terminal;

a fourteenth MOS transistor with a first terminal connected to the first terminal of the ~~aforementioned~~ fourth capacitor element and a second terminal connected to the ~~aforementioned~~ voltage output terminal;

a fifteenth MOS transistor with a first terminal connected to the first terminal of the ~~aforementioned~~ second capacitor and a second terminal connected to the ~~aforementioned~~ voltage output terminal;

~~the switching control means controls as follows:~~

in the first phase, the switching controller keeps the first, second, fourth, sixth, ninth, eleventh, and fifteenth MOS transistors ~~are kept~~ in the on state, and the third, fifth, seventh, eighth, tenth, twelfth, thirteenth, and fourteenth MOS transistors ~~are kept~~ in the off state;

in the second phase, the switching controller keeps the first, second, fourth, sixth, ninth, eleventh, and fifteenth MOS transistors ~~are kept~~ in the off state, and the third, fifth, seventh, eighth, tenth, twelfth, thirteenth, and fourteenth MOS transistors ~~are kept~~ in the on state.

18. (currently amended) The DC/DC converter described in ~~any of Claims 1-17 characterized by having~~ Claim 1 further comprising a third capacitor for smoothing with a first terminal connected to the ~~aforementioned~~ voltage output terminal and a second terminal connected to the reference potential.

19. (currently amended) The DC/DC converter described in ~~any of Claims 1-18 characterized by having the following:~~ Claim 1 wherein

a current control circuit that is connected in series between the ~~aforementioned~~ voltage input terminal and the ~~aforementioned~~ first capacitor,

a voltage ~~detecting means~~ detector is used for detecting the output voltage obtained at the ~~aforementioned~~ voltage output terminal,

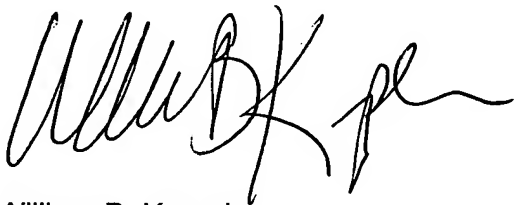
a reference voltage ~~generating means~~ generator that can ~~generate~~ generates a reference voltage corresponding to the set value of the output voltage output from the ~~aforementioned~~ voltage output terminal, and

a current ~~control means that~~ controller compares the ~~aforementioned~~ output voltage detected by the ~~aforementioned~~ voltage ~~detecting means~~ detector with the ~~aforementioned~~

reference voltage and controls the current ~~of~~ in the ~~aforementioned~~ current control circuit corresponding to the comparison error.

20. The DC/DC converter described in ~~any of Claims 5, 9, 13, 17 characterized by the fact that~~ Claim 5 wherein all of the ~~aforementioned~~ MOS transistors are turned off simultaneously in the phase switching period between the ~~aforementioned~~ first and second phases.

Respectfully submitted,



William B. Kempler
Senior Corporate Patent Counsel
Reg. No.: 28,228

Texas Instruments Incorporated
P. O. Box 655474, MS 3999
Dallas, Texas 75265
(972) 917-5452
Fax: 972-917-4418